CLAIMS

What is claimed is:

1. An interface between a master device and a slave device, said interface comprising a bit serial bidirectional signal line for conveying commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

2. An interface as in claim 1, where said master device is comprised of a personal digital assistant.

3. An interface as in claim 1, where said master device is comprised of a mobile terminal.

4. An interface as in claim 3, where said mobile terminal samples the data transferred from said slave device to said master device at a rate established by a mobile terminal sleep clock.

5. An interface as in claim 1, where said interface comprises, in said slave device, an Accessory Control Interface chip and an oscillator providing a clock signal to said Accessory Control Interface chip, where the bit time is a multiple of the clock signal, and where said master device adapts the sampling of the data transferred from said slave device in accordance with the specified duration of the bit time.

6. An interface as in claim 1, where said interface comprises, in said slave device, an Accessory Control Interface chip and a non-volatile memory for storing slave device related feature data that is readable by said master device over said bit serial bidirectional signal line in response to a memory read command sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line.

7. An interface as in claim 1, where said interface comprises, in said slave device, an

Accessory Control Interface chip and a challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line, and where authentication result data is sent by said Accessory Control Interface chip to said master device over said bit serial bidirectional signal line in response to an authentication result command sent from said master device to said Accessory Control Interface chip over said bit serial bidirectional signal line.

8. An interface as in claim 1, where said bit serial bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

9. An interface circuit for coupling a slave device to a master device, said interface circuit supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal, an interrupt signal, and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

10. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises an oscillator for generating a clock signal, where the bit time is a multiple of the clock signal period, and where said master device samples said bit serial bidirectional signal line in accordance with the specified duration of the bit time.

11. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises a non-volatile memory for storing slave device related feature data that is readable by said master device over said bit serial bidirectional signal line in response to a read command sent from said master device to said interface circuit over said bit serial bidirectional signal line.

12. An interface circuit as in claim 9, where said interface circuit is disposed within said slave device and comprises a challenge/response authentication function that is challenged in response to an authentication challenge command and associated challenge data received from said master device over said bit serial bidirectional signal line, and

where authentication result data is sent to said master device over said bit serial bidirectional signal line in response to receiving an authentication result command from said master device over said bit serial bidirectional signal line.

13. An interface circuit as in claim 9, where said bit serial bidirectional signal line further conveys a slave device connected/disconnected state to said master device.

14. An interface circuit as in claim 9, where said master device is comprised of a mobile terminal.

15. An interface circuit as in claim 14, where said mobile terminal samples said bit serial bidirectional signal line at a rate established by a mobile terminal sleep clock.

16. An interface circuit as in claim 9, where said master device is comprised of a personal digital assistant.

17. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a reset signal.

18. An interface circuit as in claim 17, where said other signals further comprise an interrupt signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

19. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising an interrupt signal.

20. An interface circuit as in claim 19, where said other signals further comprise a reset

signal and a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

21. An interface circuit for coupling a slave device to a master device, said interface circuit being disposed in said slave device and supporting a bit serial bidirectional signal line that conveys commands and associated data from said master device to said slave device, said bit serial bidirectional signal line further conveying other signals, said other signals comprising a learning sequence signal for specifying a duration of a bit time for data transferred from said slave device to said master device.

22. An interface circuit as in claim 21, where said interface circuit comprises an oscillator for generating a clock signal, where the duration of the bit time is a multiple of the clock signal period, and where said master device samples said bit serial bidirectional signal line in accordance with the specified duration of the bit time.

23. An interface circuit as in claim 22, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on said bit serial bidirectional signal line by a predetermined point in the specified duration of the bit time.

24. An interface circuit as in claim 23, where the specified duration of the bit time is given by T, and where the predetermined point is about T/2.

25. An interface circuit as in claim 21, where said interface circuit comprises at least one register that is readable by said master device over said bit serial bidirectional signal line.

26. An interface circuit as in claim 21, where said interface circuit comprises at least one register that is writable by said master device over said bit serial bidirectional signal line.

27. An interface circuit as in claim 21, where said interface circuit comprises at least one memory device location that is readable by said master device over said bit serial bidirectional signal line.

28. An interface circuit as in claim 21, where said interface circuit comprises at least one

memory device location that is writable by said master device over said bit serial bidirectional signal line.

29. An interface circuit as in claim 21, where said interface circuit comprises an authentication block that is addressable by commands sent by said master device over said bit serial bidirectional signal line, and that responds to at least one command with response data sent to said master device over said bit serial bidirectional signal line.

30. An interface circuit as in claim 21, where said other signals further comprise a reset signal and an interrupt signal.

31. A method for communicating between a master device and a slave device, comprising:

coupling the slave device to the master device through an interface, the interface comprising a bit serial bidirectional signal line;

sending a reset signal from the master device to the slave device over the bit serial bidirectional signal line;

sending a learning sequence signal to the master device over the bit serial bidirectional signal line for specifying a duration of a bit time for data transferred between the master device and the slave device; and

communicating at least one of data and commands between the master device and the slave device over the bit serial bidirectional signal line.

32. A method as in claim 31, where communicating comprises the master device sampling the bit serial bidirectional signal line in accordance with the specified duration of the bit time.

33. A method as in claim 32, where a logic zero and a logic one are distinguished by a presence or absence of a transition occurring on the bit serial bidirectional signal line by

a predetermined point in the specified duration of the bit time.

34. A method as in claim 33, where the specified duration of the bit time is given by T, and where the predetermined point is about T/2.